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DATA SHEET

TEA1207T
High efficiency DC/DC converter

Preliminary specification
Supersedes data of 1999 Jan 14
File under Integrated Circuits, IC03

1999 Oct 21

Philips
Semiconductors

PHILIPS

High efficiency DC/DC converter TEA1207T

FEATURES

- Fully integrated DC/DC converter circuit
- Up-or-down conversion
- Start-up from 1.85 V input voltage
- Adjustable output voltage
- High efficiency over large load range
- Power handling capability up to 0.85 A continuous average current
- 275 kHz switching frequency
- Low quiescent power consumption
- Synchronizing with external clock
- True current limit for Li-ion battery compatibility
- Up to 100% duty cycle in down mode
- Undervoltage lockout
- Shut-down function
- 8-pin SO package.

APPLICATIONS

- Cellular and cordless phones, Personal Digital Assistants (PDAs) and others
- Supply voltage source for low-voltage chip sets
- Portable computers
- Battery backup supplies
- Cameras.

GENERAL DESCRIPTION

The TEA1207T is a fully integrated DC/DC converter. Efficient, compact and dynamic power conversion is achieved using a novel digitally controlled concept like Pulse Width Modulation (PWM) or Pulse Frequency Modulation (PFM), integrated low R_{DSon} CMOS power switches with low parasitic capacitances, and fully synchronous rectification.

The device operates at 275 kHz switching frequency which enables the use of external components with minimum size. Deadlock is prevented by an on-chip undervoltage lockout circuit.

Efficient behaviour during short load peaks and compatibility with Li-ion batteries is guaranteed by an accurate current limiting function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1207T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
UPCONVERSION; pin $\overline{U}$/D = LOW						
V_I	input voltage		$V_{I(start)}$	–	5.50	V
V_O	output voltage		2.80	–	5.50	V
$V_{I(start)}$	start-up input voltage	I_L < 125 mA	1.40	1.60	1.85	V
DOWNCONVERSION; pin $\overline{U}$/D = HIGH						
V_I	input voltage		2.80	–	5.50	V
V_O	output voltage		1.30	–	5.50	V
GENERAL						
V_{fb}	feedback voltage		1.19	1.24	1.29	V
Current levels						
I_q	quiescent current on pin 3	down mode; V_I = 3.6 V	52	65	72	µA
I_{shdwn}	current in shut-down state		–	2	10	µA
I_{LX}	maximum continuous current on pin 4	T_{amb} = 80 °C	–	–	0.60	A
ΔI_{lim}	current limit deviation	I_{lim} = 0.5 to 5 A				
		up mode	–17.5	–	+17.5	%
		down mode	–17.5	–	+17.5	%
Power MOSFETs						
R_{DSon}	drain-to-source on-state resistance					
	N-type		0.10	0.20	0.30	Ω
	P-type		0.10	0.22	0.35	Ω
Efficiency						
η_1	efficiency upconversion	V_I = 3.6 V; V_O = 4.6 V; L1 = 10 µH				
		I_L = 1 mA	–	88	–	%
		I_L = 200 mA	–	95	–	%
		I_L = 1 A; pulsed	–	83	–	%
η_2	efficiency downconversion	V_I = 3.6 V; V_O = 2.0 V; L1 = 10 µH				
		I_L = 1 mA	–	86	–	%
		I_L = 200 mA	–	93	–	%
		I_L = 1 A; pulsed	–	81	–	%
Timing						
f_{sw}	switching frequency	PWM mode	220	275	330	kHz
f_{sync}	synchronization clock input frequency		4	6.5	20	MHz
t_{res}	response time	from standby to $P_{0(max)}$	–	50	–	µs

BLOCK DIAGRAM

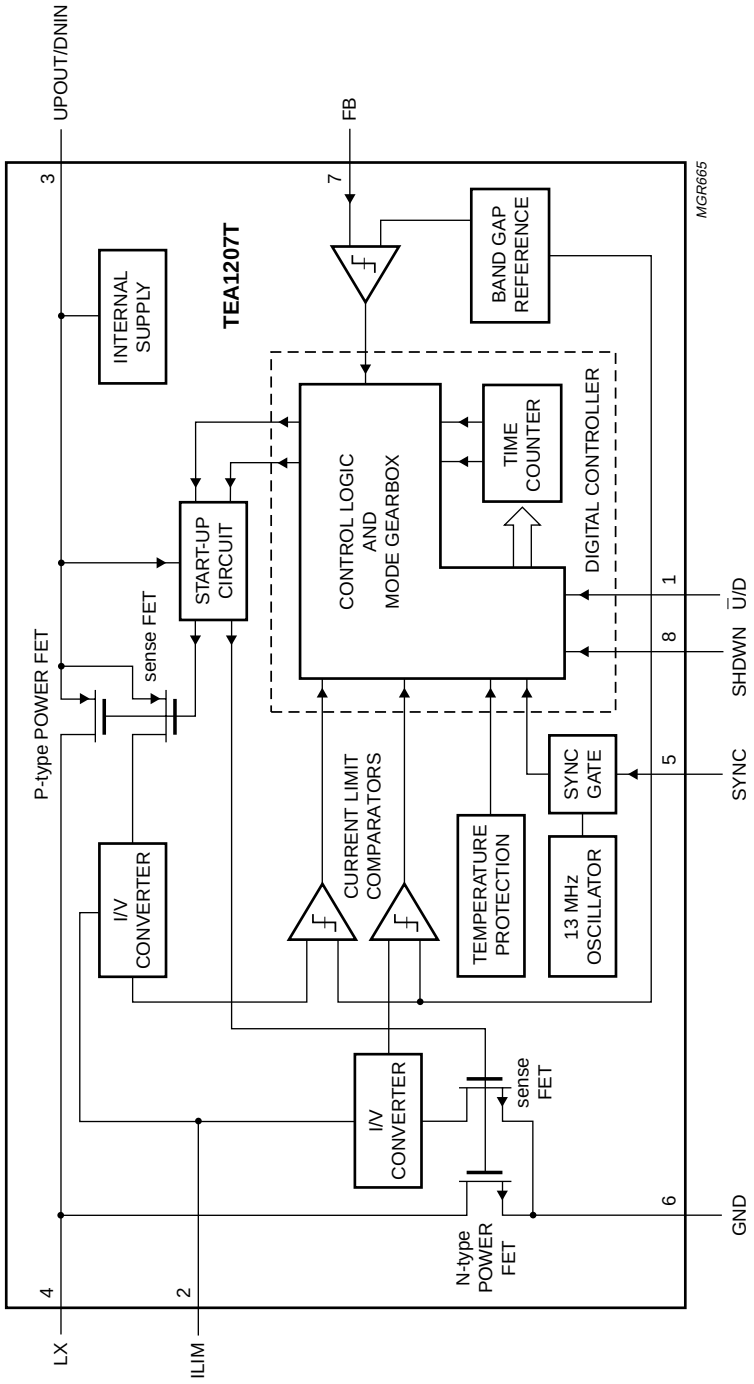


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{U}$/D	1	up-or-down mode selection input; active LOW for up mode
ILIM	2	current limiting resistor connection
UPOUT/DNIN	3	output voltage in up mode; input voltage in down mode
LX	4	inductor connection
SYNC	5	synchronization clock input
GND	6	ground
FB	7	feedback input
SHDWN	8	shut-down input

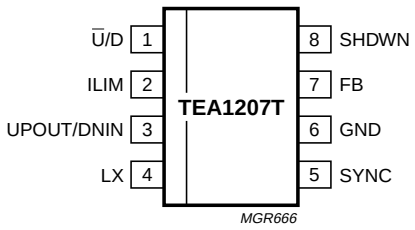


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Control mechanism

The TEA1207T DC/DC converter is able to operate in PFM (discontinuous conduction) or PWM (continuous conduction) operating mode. All switching actions are completely determined by a digital control circuit which uses the output voltage level as its control input. This novel digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete operating range of the converter.

When high output power is requested, the device will operate in PWM (continuous conduction) operating mode. This results in minimum AC currents in the circuit components and hence optimum efficiency, minimum costs and low EMC. In this operating mode, the output voltage is allowed to vary between two predefined voltage levels. As long as the output voltage stays within this so-called window, switching continues in a fixed pattern. When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the pulse width and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations. Figure 3 shows the converter's response to a sudden load increase. The upper trace shows the output voltage. The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, times the capacitor's internal Equivalent Series Resistance (ESR). After each ramp-down of the inductor current, i.e. when the ESR effect increases the output voltage, the converter determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay.

When the output voltage becomes lower than the low limit of the window, a corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue. The output voltage (including ESR effect) is again within the predefined window. Figure 4 depicts the spread of the output voltage window. The absolute value is most dependent on spread, while the actual window size is not affected. For one specific device, the output voltage will not vary more than 2% typically.

In low output power situations, the TEA1207T will switch over to PFM (discontinuous conduction) operating mode. In this mode, regulation information from earlier PWM operating modes is used. This results in optimum inductor peak current levels in the PFM mode, which are slightly larger than the inductor ripple current in the PWM mode. As a result, the transition between PFM and PWM mode is optimum under all circumstances. In the PFM mode the TEA1207T regulates the output voltage to the high window limit as shown in Fig.3.

Synchronous rectification

For optimum efficiency over the whole load range, synchronous rectifiers inside the TEA1207T ensure that during the whole second switching phase, all inductor current will flow through the low-ohmic power MOSFETs. Special circuitry is included which detects that the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds regulation.

Start-up

Start-up from low input voltage in boost mode is realized by an independent start-up oscillator, which starts switching the N-type power MOSFET as soon as the voltage at pin UPOUT/DNIN is measured to be sufficiently high. The switch actions of the start-up oscillator will increase the output voltage. As soon as the output voltage is high enough for normal regulation, the digital control system takes over the control of the power MOSFETs.

Undervoltage lockout

As a result of too high load or disconnection of the input power source, the output voltage can drop so low that normal regulation cannot be guaranteed. In that case, the device switches back to start-up mode. If the output voltage drops down even further, switching is stopped completely.

Shut-down

When the shut-down input is made HIGH, the converter disables both power switches and the power consumption is reduced to a few microamperes.

Power switches

The power switches in the IC are one N-type and one P-type power MOSFET, having a typical drain-to-source resistance of 0.20 Ω and 0.22 Ω respectively.
The maximum average current in the power switches is 0.60 A at T_{amb} = 80 °C.

Temperature protection

When the device operates in PWM mode, and the die temperature gets too high (typically 175 °C), the converter stops operating. It resumes operation when the die temperature falls below 175 °C again. As a result, low-frequent cycling between the on and off state will occur. It should be noted that in the event of a device temperature around the cut-off limit, the application differs strongly from maximum specifications.

Current limiters

If the current in one of the power switches exceeds its limit in the PWM mode, the current ramp is stopped immediately, and the next switching phase is entered. Current limiting is required to enable optimal use of energy in Li-ion batteries, and to keep power conversion efficient during temporary high loads. Furthermore, current limiting protects the IC against overload conditions, inductor saturation, etc. The current limiting level is set by an external resistor.

External synchronization

If an external high-frequency clock is applied to the synchronization clock input, the switching frequency in PWM mode will be exactly that frequency divided by 22. In the PFM mode, the switching frequency is always lower. The quiescent current of the device increases when external clock pulses are applied. In case no external synchronization is necessary, the synchronization clock input must be connected to ground level.

Behaviour at input voltage exceeding the specified range

In general, an input voltage exceeding the specified range is not recommended since instability may occur. There are two exceptions:

- Upconversion: at an input voltage higher than the target output voltage, but up to 6 V, the converter will stop switching and the internal P-type power MOSFET will be conducting. The output voltage will equal the input voltage minus some resistive voltage drop. The current limiting function is not active.
- Downconversion: when the input voltage is lower than the target output voltage, but higher than 2.8 V, the P-type power MOSFET will stay conducting resulting in an output voltage being equal to the input voltage minus some resistive voltage drop. The current limiting function remains active.

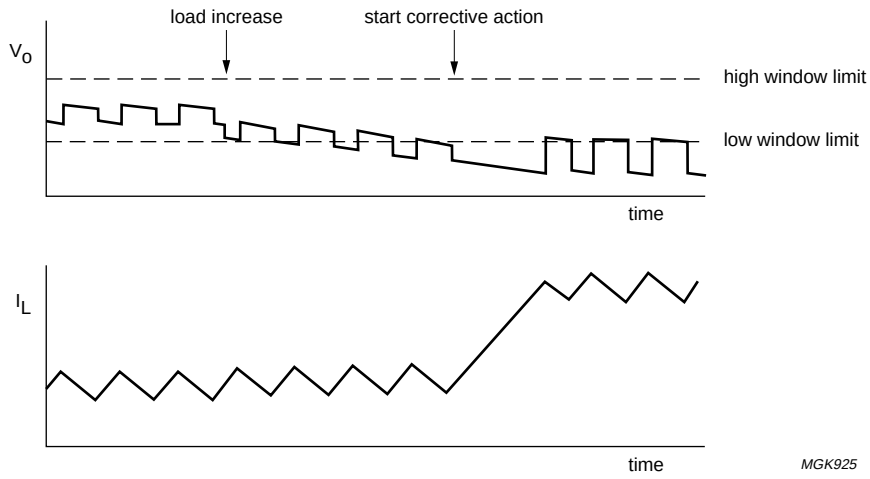


Fig.3 Response to load increase.

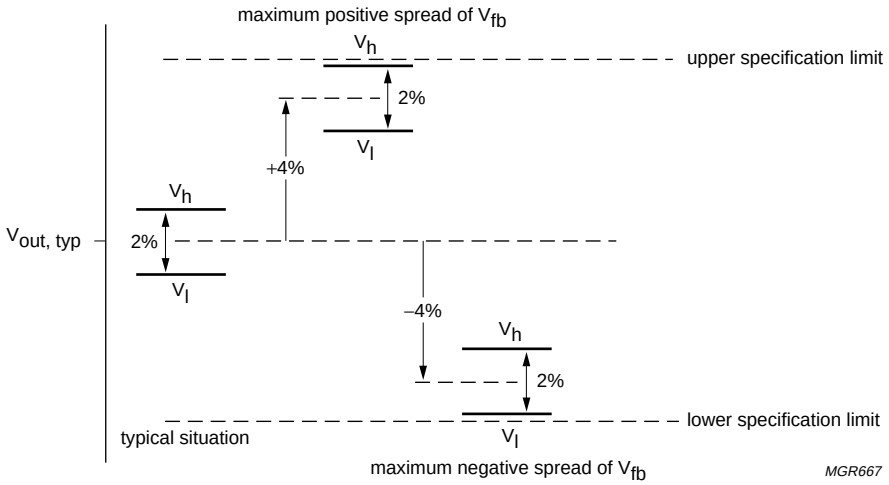


Fig.4 Spread of location of output voltage window.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any pin	shut-down mode	–0.2	+6.5	V
		operating mode	–0.2	+5.9	V
T_j	junction temperature		–25	+150	°C
T_{amb}	ambient temperature		–40	+80	°C
T_{stg}	storage temperature		–40	+125	°C
V_{es}	electrostatic handling voltage	human body model; note 1	–4000	+4000	V
		machine model; note 2	–300	+300	V

Notes

1. Class 3; equivalent to discharging a 100 pF capacitor through a 1500 resistor.
2. Class 2; equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	150	K/W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611 part E”*.

CHARACTERISTICS

T_{amb} = –40 to +80 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
UPCONVERSION; pin $\overline{U}$/D = LOW						
V_I	input voltage		$V_{I(start)}$	–	5.50	V
V_O	output voltage		2.80	–	5.50	V
$V_{I(start)}$	start-up input voltage	I_L < 125 mA	1.40	1.60	1.85	V
$V_{I(uvlo)}$	undervoltage lockout input voltage	note 1	1.50	2.10	2.50	V
DOWNCONVERSION; PIN $\overline{U}$/D = HIGH						
V_I	input voltage	note 2	2.80	–	5.50	V
V_O	output voltage		1.30	–	5.50	V
GENERAL						
V_{fb}	feedback input voltage		1.19	1.24	1.29	V
ΔV_{wdw}	output voltage window	PWM mode	1.5	2.0	3.0	%
Current levels						
I_q	quiescent current on pin 3	down mode; V_3 = 3.6 V; note 3	52	65	72	µA
I_{shdwn}	current in shut-down mode		–	2	10	µA
I_{LX}	maximum continuous current on pin 4	T_{amb} = 60 °C	–	–	0.85	A
		T_{amb} = 80 °C	–	–	0.60	A
ΔI_{lim}	current limit deviation	I_{lim} = 0.5 to 5.0 A; note 4				
		up mode	–17.5	–	+17.5	%
		down mode	–17.5	–	+17.5	%
Power MOSFETs						
R_{DSon}	drain-to-source on-state resistance					
	N-type		0.10	0.20	0.30	Ω
	P-type		0.10	0.22	0.35	Ω
Efficiency						
η_1	efficiency upconversion	V_I = 3.6 V; V_O = 4.6 V; L1 = 10 µH; note 5				
		I_L = 1 mA	–	88	–	%
		I_L = 10 mA	–	93	–	%
		I_L = 50 mA	–	93	–	%
		I_L = 100 mA	–	94	–	%
		I_L = 200 mA	–	95	–	%
		I_L = 500 mA	–	92	–	%
		I_L = 1 A; pulsed	–	83	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
η_2	efficiency downconversion	V_I = 3.6 V; V_O = 2.0 V; L1 = 10 µH; note 5				
		I_L = 1 mA	–	86	–	%
		I_L = 10 mA	–	91	–	%
		I_L = 50 mA	–	92	–	%
		I_L = 100 mA	–	92	–	%
		I_L = 200 mA	–	93	–	%
		I_L = 500 mA	–	89	–	%
		I_L = 1 A; pulsed	–	81	–	%
Timing						
f_{sw}	switching frequency	PWM mode	220	275	330	kHz
f_{sync}	synchronization clock input frequency		4	6.5	20	MHz
t_{res}	response time	from standby to $P_{o(max)}$	–	50	–	µs
Temperature						
T_{amb}	ambient temperature		–40	+25	+80	°C
T_{max}	internal cut-off temperature		150	175	200	°C
Digital levels						
V_{IL}	LOW-level input voltage on pins 1, 5 and 8		0	–	0.4	V
V_{IH}	HIGH-level input voltage	note 6				
	on pin 1		V_3 – 0.4	–	V_3 + 0.3	V
	on pins 5 and 8		0.55V_3	–	V_3 + 0.3	V

Notes

1. The undervoltage lockout voltage shows wide specification limits since it decreases at increasing temperature. When the temperature increases, the minimum supply voltage of the digital control part of the IC decreases and therefore the correct operation of this function is guaranteed over the whole temperature range.
2. When V_I is lower than the target output voltage but higher than 2.8 V, the P-type power MOSFET will remain conducting (100% duty cycle), resulting in V_O following V_I.
3. V_3 is the voltage on pin 3 (UPOUT/DNIN).
4. The current limit is defined by an external resistor R_{lim} (see Section “Current limiting resistors”). Accuracy of the current limit increases in proportion to the programmed current limiting level.
5. The specified efficiency is valid when using an output capacitor having an ESR of 0.10 Ω and a 10 µH small size inductor (Coilcraft DT1608C-103).
6. If the applied HIGH-level voltage is less than V_3 – 1 V, the quiescent current (I_q) of the device will increase.

APPLICATION INFORMATION

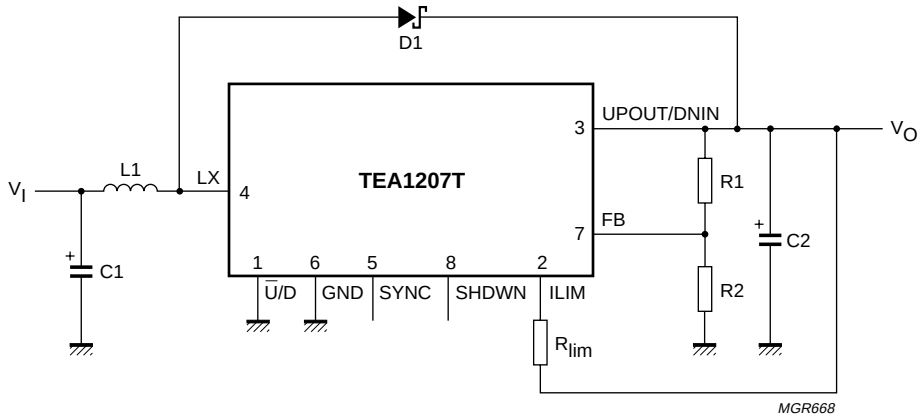


Fig.5 Complete application diagram for upconversion.

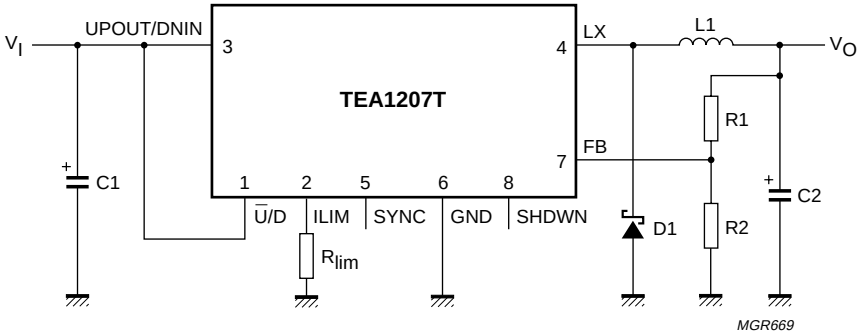


Fig.6 Complete application diagram for downconversion.

External component selection

INDUCTOR L1

The performance of the TEA1207T is not very sensitive to the inductance value. Best efficiency performance over a wide load current range is achieved by using e.g. TDK SLF7032-6R8M1R6, having an inductance of 6.8 μH and a saturation current level of 1.6 A. In case the maximum output current is lower, other inductors are also suitable such as the small sized Coilcraft DT1608 range.

INPUT CAPACITOR C1

The value of capacitor C1 strongly depends on the type of input source. In general, a 100 μF tantalum capacitor will do, or a 10 μF ceramic capacitor featuring very low series resistance (ESR value).

OUTPUT CAPACITOR C2

The value and type of capacitor C2 depend on the maximum output current and the ripple voltage which is allowed in the application. Low-ESR tantalum as well as ceramic capacitors show good results. The most important specification of capacitor C2 is its ESR, which mainly determines the output voltage ripple.

DIODE D1

The Schottky diode is only used a short time during takeover from N-type power MOSFET and P-type power MOSFET and vice versa. Therefore, a medium-power diode such as Philips PRLL5819 is sufficient.

FEEDBACK RESISTORS R1 AND R2

The output voltage is determined by the resistors R1 and R2. The following conditions apply:

- Use 1% accurate SMD type resistors only. In case larger body resistors are used, the capacitance on pin 7 (feedback input) will be too large, causing inaccurate operation.
- Resistors R1 and R2 should have a maximum value of 50 kΩ when connected in parallel. A higher value will result in inaccurate operation.

Under these conditions, the output voltage can be calculated by the formula: $V_O = 1.24 \times \left(1 + \frac{R1}{R2}\right)$

CURRENT LIMITING RESISTORS

The maximum instantaneous current is set by the external resistor R_{lim}. The preferred type is SMD, 1% accurate. The connection of resistor R_{lim} differs per mode:

- At upconversion (up mode): resistor R_{lim} must be connected between pin 2 (ILIM) and pin 3 (UPOUT/DNIN).

  The current limiting level is defined by: $I_{lim} = \frac{238}{R_{lim}}$

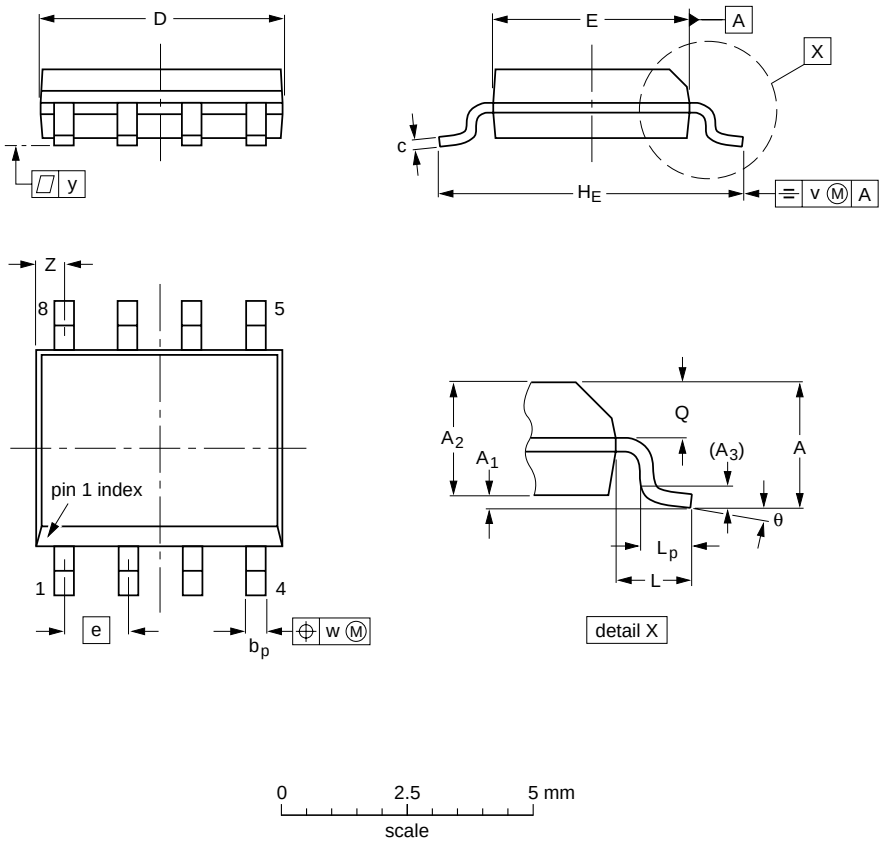
- At downconversion (down mode): resistor R_{lim} must be connected between pin 2 (ILIM) and pin 6 (GND).

  The current limiting level is defined by: $I_{lim} = \frac{270}{R_{lim}}$

The average inductor current during limited current operation also depends on the inductance value, input voltage, output voltage and resistive losses in all components in the power path. Ensure that $I_{lim} < I_{sat}$ (saturation current) of the inductor.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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